D. REMARKS

Claims 1-12, 14-19, 24, and 25 are pending in the present application. Claims 13 and 20-23 have been cancelled. Claims 14 and 25 have been amended. Reconsideration of the claims is respectfully requested.

Objection to Title

The Examiner objected to the title of the invention as lacking the requisite level of descriptiveness. In response, Applicants have amended the title to read "**Memory Allocation Using Mask-Bit Pattern to Encode Metadata within Memory Address**," per the Examiner's suggestion. Applicants therefore respectfully request withdrawal of the objection.

35 U.S.C. § 101, Subject Matter

The Examiner rejected claims 20-23 and 25 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. As Applicants have cancelled claims 20-23, the rejection of those claims is now moot.

With respect to claim 25, the Examiner argues that the claim, if read broadly, encompasses non-tangible or ephemeral phenomena, such as electromagnetic signals, that fall outside of the scope of patentable subject matter under 35 U.S.C. § 101.

Without necessarily agreeing that the Examiner's rejection has merit, Applicants have amended claim 25 to recite a computer program product in a "tangible, computer-readable medium" containing "functional descriptive material that, when executed by a computer, directs the computer to perform" particular actions. "Functional descriptive material" consists of data structures and computer programs that impart functionality when employed as a computer component. MPEP § 2106. When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. *Id.*; *In re Lowry*, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994).

Accordingly, claim 25, at least as amended, is directed to a computer program product that is statutory in scope inasmuch as it is a tangible article of manufacture containing functional descriptive material that imparts functionality to a computer. Applicants therefore respectfully request that the rejection of claim 25 be withdrawn.

35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-3, 8-12, 15-16, 19, and 25 under 35 U.S.C. § 102 as being anticipated by *Kobayashi* (U.S. Patent No. 5,706,469). This rejection is respectfully traversed.

With respect to independent claim 1, the rejection of which is representative of the rejections of the other independent claims, the Examiner stated:

> As per claims 1, 15, 20-23 and 25 Kobayashi discloses "A method/mechanism of allocating memory in a data processing system having a memory, the method comprising the steps of:" as ["a data processing system capable of controlling bus access to a memory area of an arbitrary size with the use of a small number of registers" (Column 2, lines 19-21)] "receiving a memory allocation request from a running process, the request including data relating to the size of the block of memory required and an indication of a mask bit pattern;" [Kobayashi discloses this concept as "the microprocessor 1, whenever it becomes necessary to make access to memory 3, sends information required for the access including an access request generated in an internal data arithmetic section or the like together with the address, data length, direction of transfer (read/write) and, appropriate data in the case of a write cycle" (Column 8, lines 60-66) and explains that "a signal indicating that the most significant bits in the to-be-accessed address which are not masked by the mask bits coincide with the most significant bits of the head address set in the memory area address register is output to the memory controller decoding the address as a signal for specifying the memory area to be accessed" (Column 2, lines 53.59); wherein "as a result, the head address of the memory area of a size designated by the mask bits and containing the address to be accessed is extracted from the particular address" (Column 9, lines 18.21) as having both, a size of a memory block to be accessed and mask bit pattern within a memory allocation request "selecting a block of memory of appropriate size and having an address including a bit pattern corresponding correctly to the mask bit pattern; and allocating the selected block of memory to the process" [With respect to this limitation, Kobayashi discloses having EX-NOR gates to check whether masked bits coincide with a memory address register (Column 9, lines 22-34); providing an example in which a "to-be-accesses address" corresponds to area I on the memory space and explains that "the memory controller 2" decodes the most significant 4 bits of the to-be-accessed address wherein "a MEM(1)# signal means that the most significant four bits of the address coincide with the most significant four bits of the memory are address register (1)" (Column 9, lines 45- 57) as providing the necessary steps for selecting a memory are to be accessed].

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as

they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). *Kobayashi* fails to anticipate the presently claimed invention because it fails to show all of the elements of the claimed invention.

The rejected independent claims, 1, 15, and 25, all recite "receiving a memory allocation request from a running process, the request including data relating to the size of the block of memory required and an indication of a mask bit pattern." This feature is not taught by *Kobayashi*.

Unlike the present invention, *Kobayashi* does not deal with memory allocation or memory management. *Kobayashi* is directed to the interfacing of hardware memory components over a computer bus. While *Kobayashi* does employ a mask bit pattern, it does so in the context of memory controller hardware, in which the sizes of the memory areas corresponding to different parts of the memory hardware are indicated using a mask register. Other information needed to interface with the memory hardware (such as the number of wait states needed, for example) are stored in a corresponding memory address register:

> 0-10th bits of the memory area address register are assigned to the most significant 20 MAD(0:19) bits (first bit string) of the head address of each of memory areas 0 to 3; 22nd bit is assigned to an EXT bit (0: invalid, 1: valid) (fourth bit) indicating whether the external input signal check mode is to be set to refer to the external input signal from the memory controller 2; 23rd bit is assigned to a BE bit (0: No, 1: Yes) (sixth bit) indicating the presence or absence of a bus error; 24-28th bits are assigned to NW(0:4) bits (second bit string) indicating the number of waits (0:31) for the single cycle; 20-80th bits are assigned to BW(0:1) bits (second bit string) indicating the number of waits (0:3) for the burst cycle; and 31st bit is assigned to a BM bit (0: No, 1: Yes) indicating the presence or absence of a burst transfer.
>
> In bits 0 to 19 of the memory area mask register are assigned mask bits (third bit string) for masking a predetermined number of least significant ones of the most significant 20 bits of the address to be accessed in accordance with the size of the memory area to be designated and thus specifying the size of memory areas 0 to 3. According to this embodiment, an area of 4 KB can be designated if the mask bits are all set to 1'B. In the case where all the mask bits are set to 0'B, an area of 4 GB can be designated, so that a memory area of an arbitrary size can be designated in the range of 4 GB to 4 KB with mask bits of 00000'H to 11111'H ('H hereinafter denotes a hexadecimal number). [col. 7, line 66 – col 8, line 13].

Kobayashi neither teaches nor suggests Applicants' claimed feature of a receiving a memory allocation request. The *Kobayashi* invention does not receive or process allocation requests, because *Kobayashi* deals only with the hardware interfacing of memory components and not with the allocation of memory for use by software.

Moreover, the *Kobayashi* invention, being a low-level hardware system, should ideally operate transparently with respect to the software executing on the computer system. Thus, there is no reason why the *Kobayashi* invention would ever receive an allocation request *from a running process*. The processes running on a computer system constructed in accordance with *Kobayashi* would have no way of issuing allocation requests to *Kobayashi*'s hardware system, because *Kobayashi's* hardware system would be transparent to any such process. Therefore, not only does *Kobayashi* not teach receiving an allocation request from a running process, but one skilled in the art would not have a motivation or incentive to modify *Kobayashi* to do so, since *Kobayashi*'s memory hardware is ideally transparent to software.

Further, nowhere does *Kobayashi* mention any kind of request that contains both a block size and a mask bit pattern. The only mask bit pattern described in *Kobayashi* is that stored in the memory area mask register. *Kobayashi*'s mask bit pattern never forms any part of a request; it is merely stored in the appropriate register in the memory controller. Hence, *Kobayashi* fails to teach or suggest all of the elements of independent claims 1, 15, and 25.

Claims 2-3, 8-12, 16, and 19 are dependent claims that depend from independent claims 1, 15, and 25. Applicants have already demonstrated claims 1, 15, and 25 to be in condition for allowance. Applicants respectfully submit that claims 2-3, 8-12, 16, and 19 are also allowable, at least by virtue of their dependency on allowable claims.

Accordingly, Applicants respectfully request that the rejection of claims 1-3, 8-12, 15-16, 19, and 25 be withdrawn.

35 U.S.C. § 103, Obviousness

Claim 4

The Examiner rejected claim 4 under 35 U.S.C. § 103 as being obvious in view of *Kobayashi* and *Kirk III* (U.S. Patent 6,421,690). This rejection is respectfully traversed.

Claim 4 is a dependent claim that depends from independent claim 1. *Kirk III* fails to cure the deficiencies of *Kobayashi* with respect to the features of claim 1 that are contained in

claim 4 by dependency. Specifically, *Kirk III* fails to teach or suggest the claimed feature of receiving a memory allocation request from a running process, where the request includes data relating to the size of the block of memory required *and* an indication of a mask bit pattern. Thus claim 4 is patentable over the cited references for at least the reasons set forth with respect to independent claim 1.

Moreover, *Kirk III* fails to teach the claimed feature of "embedding one or more bits of metadata into the address of the allocated block of memory." While the Examiner correctly notes that *Kirk III* teaches a type of enhanced pointer data structure in which additional information is stored in the pointer data structure in addition to a memory address, *Kirk III* differs from the present invention as recited in claim 4, because *Kirk III* teaches creating a complex pointer data structure containing additional data fields that are separate from the actual address stored in the pointer, rather than embedding metadata into the address itself. *See, e.g.,* Figure 1 of *Kirk III* and col. 5, lines 55-60 ("Referring to FIG. 1, the most preferred embodiment of GeMS smart pointer (named SmartPtr in FIG. 1) consists of four normal pointers (variables which store memory addresses) and five flags. The SmartPtr contains a standard memory pointer defining value (named 'value' in FIG. 1) which points to some external object.").

For example, if one were to declare a *Kirk III*-style pointer in C++ or a similar language, it would look something like the following:

```
struct SmartPtr {
     void *address; // Address stored here
     int flag;      // Flag stored separately
};
```

In *Kirk III*, as in the above example, "smart pointers" are multi-field data structures (*e.g., "*structs" in C or C++, "classes" in C++ and Java, "records" in Pascal, *etc.*) having separate fields for addresses and other data. To set the "flag" in the above example, one would store the flag's value in the "flag" field with a statement such as "`ptr->flag = 1`" (where "ptr" represents a pointer). Setting the flag in this way would have no effect whatsoever on the value of the address, which is stored in the separate "address" field.

In the present invention as recited in claim 4, on the other hand, metadata is actually embedded *into the address itself.* That is, the actual numerical address stored in the pointer is modified to contain the embedded metadata. One way to do this would be to set or clear one or

more bits in the address value stored by the pointer, as pointed out in Applicants' specification. *See, e.g.,* p. 19, lines 10-12, ("To set, or embed, all four flag bits in the memory address, 'Address', the process simply logical Ors them with the memory address…").

Thus *Kirk III* and *Kobayashi* not only fail to teach or suggest all of the features recited in claim 4, but *Kirk III* actually teaches away from the claimed feature of "embedding one or more bits of metadata into the address of the allocated block of memory" because it teaches a type of "smart pointer" that stores metadata separately *without* embedding the metadata into the address itself.

For the above reasons, Applicants respectfully submit that claim 4 is patentable over *Kirk III* and *Kobayashi* and request that the rejection of claim 4 be withdrawn.

Claim 5

The Examiner rejected claim 5 under 35 U.S.C. § 103 as being obvious in view of *Kobayashi, Kirk III,* and *Garthwaite* (U.S. Patent 7,016,923). This rejection is respectfully traversed.

Claim 5 is a dependent claim that depends from independent claim 1. *Kirk III* and *Garthwaite* fail to cure the deficiencies of *Kobayashi* with respect to the features of claim 1 that are contained in claim 5 by dependency. Specifically, none of these references teaches or suggest the claimed feature of receiving a memory allocation request from a running process, where the request includes data relating to the size of the block of memory required *and* an indication of a mask bit pattern. Thus claim 5 is patentable over the cited references for at least the reasons set forth with respect to independent claim 1. Applicants therefore respectfully request that the rejection of claim 5 be withdrawn.

Claims 6-7 and 17-18

The Examiner rejected claims 6-7 and 17-18 under 35 U.S.C. § 103 as being obvious in view of *Kobayashi* and *Frank* (US Patent No. 5,860,144). This rejection is respectfully traversed.

Claims 6-7 and 17-18 are dependent claims that depend from independent claims 1 and 15. *Frank* fails to cure the deficiencies of *Kobayashi* with respect to the features of claims 1 and 15 that are contained in claims 6-7 and 17-18 by dependency. Specifically, none of these references teaches or suggest the claimed feature of receiving a memory allocation request from

a running process, where the request includes data relating to the size of the block of memory required *and* an indication of a mask bit pattern. Thus claims 6-7 and 17-18 are patentable over the cited references for at least the reasons set forth with respect to independent claims 1 and 15. Applicants therefore respectfully request that the rejection of claims 6-7 and 17-18 be withdrawn.

Allowable Subject Matter

The Examiner has stated that claim 14 was objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, claim 14 has been rewritten to overcome this objection.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition for allowance, and Applicants respectfully request allowance of such claims.

Applicants respectfully request that the Examiner contact the Applicants' attorney listed below if the Examiner believes that such a discussion would be helpful in resolving any remaining questions or issues related to this Application.

Respectfully submitted,

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